A FUZZY VLSI ARCHITECTURE FOR MULTI- AND HYPERSPECTRAL IMAGE CLASSIFICATION

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Abstract. This paper describes a VLSI architecture for classification of multi- and hyperspectral imagery using Fuzzy Logic with trapezoidal membership functions. The fuzzy classifier is implemented using a rule-based approach, where each class is defined as a set of sub rules. There is only one sub rule associated to each band within a class. Each sub rule is implemented as a dedicated parallel hardware. A prototype of the proposed classifier was built using Field Programmable Gate Arrays (FPGAs) Xilinx Spartan-II. As a case study, this prototype was constructed as an eight-band image classifier capable to distinguish among four classes of interest and one rejection class.

Keywords: remote sensing, image processing, fuzzy logic, hardware.

1. Introduction

In several applications, such as pattern recognition and image classification, an application-specific hardware is desirable rather than a general-purpose hardware Hung (1995). However, a dedicated hardware is in general much more expensive than a general-purpose one. On the other hand, it is often impossible to implement high parallelism in such general-purpose hardware systems, which can be a disadvantage in real-time applications, if it is needed.

In specific cases such as remote sensing image classification, a real-time hardware classifier can reduce the time of image analysis in several engineering applications by reducing time spent in multispectral and hyperspectral image classification using parallelism.

However, the task of implementing a classical pattern recognition method like maximum likelihood Duda, Hart and Stork (2001) or others based on statistics requires, in general, adding floating-point arithmetic which increases the price of the final application due to the need of intensive computing and complex architectures. Furthermore, if we try to solve these problems by using a look-up table approach, we will need more memory units. Memory modules occupy lots of area on an electronic chip increasing, therefore, the final cost of the desired system.

In many situations, thus, an arithmetic hardware approach to implement an image classifier is more feasible and less expensive. Nevertheless, it is not completely true if we try to implement a statistics-based classifier. Hence, a classifier architecture able to work using simple hardware, basic mathematical operations and parallel structures and still achieving good classification results is highly desirable when execution time is a critical variable.

In this context, a fuzzy classifier is one of the most feasible approaches Hung (1995). A fuzzy classifier is based on Fuzzy Logic, a generalization of the Set Theory which includes the idea of sets having non-defined boundaries, called fuzzy sets Bezdek (1981).

Fuzzy classifiers are based on rules Hung, D. L. *Dedicated Digital Fuzzy Hardware*, IEEE Micro, Aug, 1995.

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Roubos (2001) that describe logic relations (intersections and unions) among the subsets in a class. Such relations are implemented by computing minimum and maximum values, which can be easily implemented in parallel hardware. It dramatically decreases required classification time and, consequently, reduces the time-to-market of the product (the image analysis).

In Fuzzy Logic, each subset within a class is associated to a fuzzy membership function, usually represented by simple functions like triangles and trapezoids Bezdek (1981). On the other hand, probability density functions are usually difficult to construct without the use of look-up tables or memory units. Furthermore, triangular and trapezoidal functions are easily computed by simple arithmetic comparisons and linear operations. Consequently, they allow a better use of area and logic blocks on a chip.

Therefore, a dedicated fuzzy hardware, despite its low level of flexibility, is probably one of the best ways to get high classification speeds at a reasonable accuracy Hung (1995). In addition, the design cost to implement fully dedicated hardware is exponentially decreasing due to the available technology of high-density configurable hardware, like FPGA (Field Programmable Gate Arrays).

This work addresses the proposal of VLSI architecture to implement a programmable fuzzy classifier based on trapezoidal membership functions to classify multi- and hyperspectral images. To validate this proposal, a fuzzy classifier was implemented in an FPGA Xilinx Spartan-II using eight spectral bands to classify in four classes of interest and a rejection class. The parameters used to describe the trapezoidal membership functions are obtained by a hardware/software codesign approach utilizing a fuzzy classification extension of ENVI implemented employing the IDL programming language, Research Systems Inc (2002).

2. Fuzzy Classification Methods

The proposed fuzzy classifier architecture employs the non-iterative methods described in Santos (2003) based on trapezoidal membership functions. Those algorithms allow multi- and hyperspectral image classification using a low cost computing approach.

A digital image $f:[0,...,m-1]\times[0,...,n-1]\rightarrow W^p$ is a function mapping a $m\times n$ grid into the p-dimensional real space. Thus, f is an image of size $m\times n$ and composed by p spectral bands. It is common to represent f by a $m\times n\times p$ matrix. Each p-dimensional element $f(i,j)$, where $0\le i\le m-1$ and $0\le j\le n-1$, is considered a p-dimensional feature vector.

Let $\mathbf{X}=(x_1,x_2,...,x_p)\in\mathbf{R}^p$ be a vector having p real features corresponding to a pixel of the image f, where the component x_j is related to the pixel value in the j-th band. Let also denote by $\Omega=(C_1,C_2,...,C_M)$ the set of the M classes present in the image. Each class C_k is associated to a *real discriminant function* $g_k:\mathbf{R}^p\times\Omega\rightarrow\mathbf{R}$ giving the degree of membership of the feature vector $\mathbf{X}$ to the class C_k, that is, "how much" $\mathbf{X}$ belongs to C_k. The classification is a decision made according to the winner class criteria Duda, Hart and Stork (2001), as follows:

$$g_k(\mathbf{X})=\max(g_1,g_2,...,g_M)\Rightarrow\mathbf{X}\in C_k \quad (1)$$

Considering $M-1$ classes of interest, we can define the M-th class as the *rejection class*. Each class C_k is composed by a set of N fuzzy rules Hung, D. L. *Dedicated Digital Fuzzy Hardware*, IEEE Micro, Aug, 1995.

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Roubos et. al. (2001) formed by A_{kj} sets, where $1 \le k \le M-1$ and $1 \le j \le N$:

$$\{x_1 \in A_{k1}\} \wedge \{x_2 \in A_{k2}\} \wedge \cdots \wedge \{x_N \in A_{kN}\} \Rightarrow \mathbf{X} \in C_k \quad (2)$$

Each A_{kj} set is associated to a *fuzzy membership function* $u_{kj} : \mathbf{R} \rightarrow [0,1]$. The membership functions represent the *degree of membership* of the value x_j to the set A_{kj}, that is, how much of the x_j component is in A_{kj}. We can see that, in the specific case of remote sensing image classification, the number of fuzzy rules defining a class, as shown in equation (2) equals p, which is the number of bands in an image.

Bezdek (1981) says that Fuzzy Logic can be considered a natural extension of Boolean algebra, where the "and" operation, denoted by "$\wedge$", is related to the minimum operation and can be associated to the intersection among sets, whereas the "or" operation, denoted by "$\vee$", is the extraction of maximum values, associated to the union among sets. Hence, the discriminant function g_k of the class C_k is defined as follows, where $1 \le k \le M-1$:

$$g_k(\mathbf{X}) = \bigwedge_{j=1}^{N} u_{kj}(x_j) \equiv \min(u_{k1}(x_1), u_{k2}(x_2), \ldots, u_{kN}(x_N)) \quad (3)$$

Where C_M is the *rejection class*. Its discriminant function g_M is obtained defining C_M as $C_M = \overline{C_1 \cup C_2 \cup \ldots \cup C_{M-1}}$. So,

$$g_M(\mathbf{X}) = 1 - \max(g_1(\mathbf{X}), g_2(\mathbf{X}), \ldots, g_{M-1}(\mathbf{X})). \quad (4)$$

The membership functions u_{kj} used here are trapezoidal and defined as follows:

$$u_{kj}(x) = \begin{cases} 0, & x < a_{kj} \vee x > d_{k,j} \\ \dfrac{(x - a_{kj})}{(b_{kj} - a_{kj})}, & a_{kj} \le x < b_{kj} \\ 1, & b_{kj} \le x \le c_{kj} \\ \dfrac{(x - d_{kj})}{(c_{kj} - d_{kj})}, & c_{kj} < x \le d_{kj} \end{cases} \quad (5)$$

Trapezoidal membership functions are used to allow capturing data asymmetry presented in data histograms within each band using the parameters a_{kj}, b_{kj}, c_{kj} and d_{kj} which are calculated by the use of several methods, like the ones described in Santos (2003).

3. Image Classification with Fuzzy Hardware

As usual, given a specific algorithm, dedicated hardware designed with a good "algorithm to architecture" mapping and appropriate technical handling always yields the highest performance Hung (1995).

This assumption is based on the allocation of optimized resources for an efficient processing and it comprises two main aspects: (i) the use of application-specific functional units, specially designed for some particular purpose and, therefore, optimized for a given data operation, and (ii) the possibility of concurrent processing through the multiple allocation of several functional units that can perform independent data dealing simultaneously.

Even though the straightforward advantages that dedicated hardware usually offers with respect to performance, the development of a specific architecture usually requires a high cost of both design and implementation, when compared to a similar software solution. This is mainly due to the low abstraction level that leads the design of optimized digital systems. Often, the desired performance is attained only when some of the well-known reductions rules of Boolean algebra can be used. At this level, a good knowledge of the technology used for the physical implementation of the design might be worthy.

The simplicity and versatility of the presented fuzzy algorithm, the advent of high-density electronic VLSI chips, the availability of programmable logic devices like FPGAs (Field Programmable Gate Arrays) and CPLDs (Configurable Programmable Logic Devices), together with the powerful high level HDLs (Hardware Description Language) and its specific tools, make dedicated digital Fuzzy hardware a feasible solution for implementing high-performance classification systems.

Making use of the VHDL (Very high speed Hardware Description Language) and the Xilinx Foundation Series tools to describe the entire design into the Spartan-II FPGA, the system was rapidly prototyped in a 200,000 equivalent gates device.

This kind of platform allows the design entry by means of textual descriptions of the modules that compose the system, following a bottom-up methodology, where the highest level modules are implemented by the connection among previous synthesized modules (lowest level macros).

The basic system macro is presented in **Figure 1**. The block denominated MBFU (Membership Functional Unit), implements the Fuzzy trapezoid membership function defined above. The MBFU is able to cope with several bands of a multispectral image, taking as input a set of data, which can be a sequence of bytes composing a pixel or a sequence of parameters describing a specific trapezoidal membership function. When we are applying a pixel in its input, the MBFU evaluates the degrees of membership for each band and each class.

For the case study presented here, eight bands of a multispectral image can be processed and classified by this module. The degrees of membership of each band are available along the eight MBFU output ports, as can be seen in **Figure 1**.

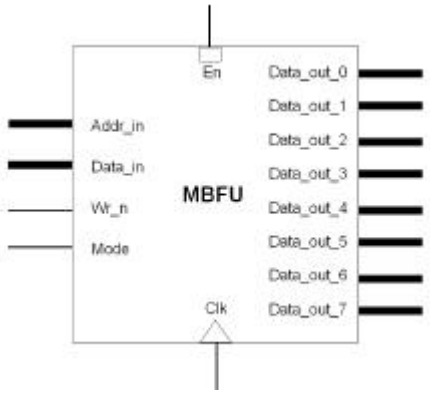

Figure 1: Membership function unit of the fuzzy classifier.

Structurally, the input and output ports available at each macrocell enable the integration among the modules and allow reaching higher system levels through the clustering of functional units.

Another macrocell, denominated MIN8, computes the intersection among the membership functions by means of a minimum operator. This module is able to perform this

operation concurrently, since the degrees of membership are all available at the MBFU output ports.

Figure 2 presents the MIN8 unit, showing its structure composed by the replication of eight lower level MIN2 macros. These latter are simple implementations of the comparison between two 8-bit values.

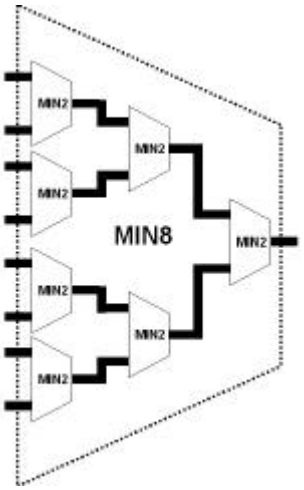

Figure 2: Functional unit that implements the minimum among eight 1-byte values.

To obtain the discriminant function of the proposed fuzzy classifier, the features of both MBFU and MIN8 modules are linked as can be seen in **Figure 3**. This arrangement was labeled as DFU (Discriminant Functional Unit).

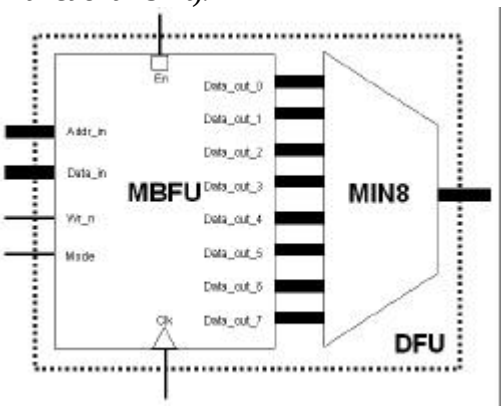

Figure 3: Discriminant functional unit

The use of several DFU modules working in parallel makes possible data classification among a variety of defined classes. In this paper, we describe the implementation of a fuzzy classifier able of distinguishing among four classes of interest and one rejection class.

According to the fuzzy classification algorithm proposed in this paper, the winner class will be the one with the highest discriminant function value or, rather, the class related to the DFU module outputting the highest value on its port.

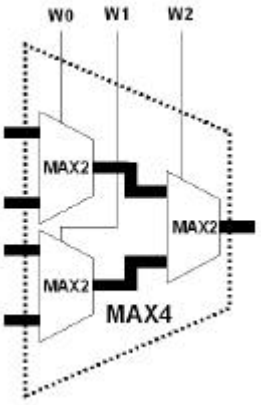

Figure 4: Maximum among four values

The maximum value among four outputs coming from DFUs can be evaluated simultaneously by means of a MAX4 unit (**Figure 4**), which is composed of three MAX2 macrocells that implement the extraction of the greatest value between two 8-bit values. Also, these modules are able to identify the winner input through the *W* binary signals, which are decoded by the Class unit.

The *Wn* signals hold the winner class index by the composition of the hierarchical comparison toward the maximum value through the modules (**Figure 4**). The class module was designed to decode the *Wn* signals, determining the class that has the greatest membership level.

The last decision is made by the REJ functional unit, which takes into account the outcome value from the MAX4 unit and rejects the classification obtained if that value is lower than half the maximum that could be reached. In our case the maximum value would be 255 (8-bit architecture). The maximum operator, the winner class decoding and the rejection analysis are grouped into the Selector unit (**Figure 5**).

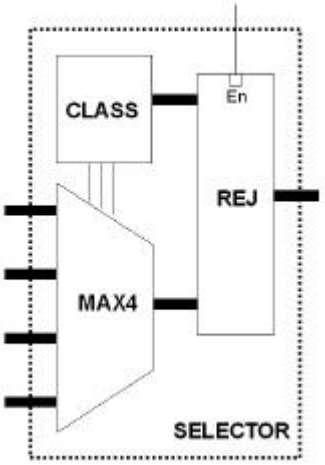

Figure 5: Selector unit including the rejection unit

The top-level system is obtained connecting the aforementioned units as shown in **Figure 6**. Such architecture is able to identify, among four distinct classes, to which class a pixel belongs to. It is made by the previous configuration of the fuzzy classifier through the provided interface (*Addr* and *Data_in* ports). When the classification process end, the classification result is presented at the host port and a interrupt signal is generated (*Int*).

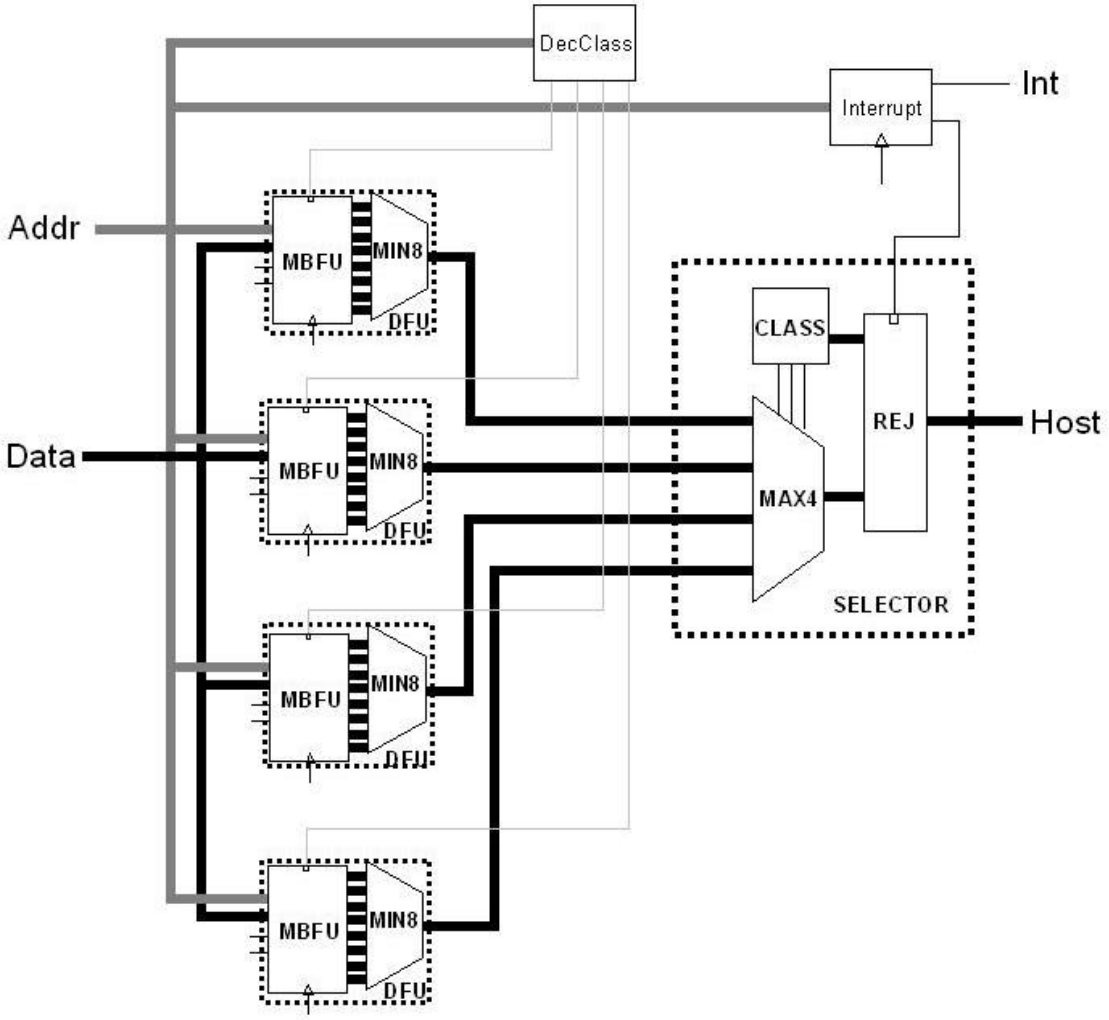

Figure 6: top level architecture of the fuzzy hardware classifier

4. Conclusions

This paper presents a dedicated fuzzy architecture proposal for multi- and hyperspectral image classification. A prototype was built using Xilinx Spartan-II FPGAs and simulations were performed using the Xilinx Foundation software. The platform was composed by a Spartan-II FPGA allocated in a PCI board able to generate interruptions to the operational system.

When the entire system was implemented into a 200,000 equivalent gates FPGA, almost 90% of the available configurable logic blocks were occupied. The maximum speed reached after classifier synthesis was about 40MHz, which is perfectly compatible with the PCI bus speed (33MHz).

There was a tight constraint imposed over the design performance requiring that the above clock frequency be only attained after skilled modifications on the VHDL code description of each module. Although the hardware abstraction brought by the use of VHDL helps reducing errors and facilitates the design stage, it turns difficult the circuit synthesis when a high level of abstraction is used.

In our case it was a serious problem. We had to use a bottom-up approach, which consists of designing the most basic modules first and, afterwards, building the more complex ones using these basic parts.

Regarding to the functionality, the architecture proposed here can be seen as a good alternative for a rapid prototyping of a fuzzy classifier. Dealing each pixel independently, the architecture is suitable to cope with images of arbitrary size, since the data is sequentially sent to the platform, allowing several formats of image inputs. This feature is seldom available in platforms that solely employ software.

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